

## RESEARCH AND CONTRIBUTIONS ABOUT THE IMPROVING OF ULTRASONIC FLAW DETECTORS PERFORMANCES

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### Abstract

This paper shows the author's preoccupations concerning the realization of a device for improving the measurement of the ultrasonic wave propagation times, which can be used as a standalone module or in combination with a ready-made cathode tube flaw detector.

**KEYWORDS:** ultrasounds, flaw detector, digital counter, quartz oscillator

### 1. INTRODUCTION

The principle of the ultrasonic flaw detection is well known: an ultrasonic pulse is emitted into the checked part, and the information about its inner flaws are obtained by studying the transformations of the signal. One important information consists of the depth at the flaw is found, which can be obtained by comparing the propagation times between the reflection on the opposite part face and on the inner flaw.

These propagation times are in the range of microseconds, which makes necessary the use of very accurate time measuring devices. The most frequent solution consists of using a cathode ray tube (CRT), where the ultrasound emission corresponds to the departure of the spot and the reception is signaled by a trace peak; the distance from the spot starting point to this peak is proportional to the ultrasound propagation time, so the distance to the reflection zone (flaw or opposite face) can be directly obtained.

This measuring method requires a grid on the CRT display, sometimes even in combination with vernier scales; even so, the reading may be affected by parallax errors, the image on the fragile CRT display may be distorted by strong external magnetic fields, and the measuring range must be permanently adapted to the operating conditions. All these disadvantages can be

minimized if the time measuring is carried out directly, with numerical display and automatic switching of the measuring range.

The device presented in this paper fulfills all these challenges, by means of usual numeric integrated circuits. The propagation time is measured by counting pulses with precise durations, emitted by a calibrated oscillator. The accuracy is given by the oscillator frequency and stability; in order to obtain 0.1  $\mu$ s precision, the clock frequency is 10 MHz. The measuring range switching is carried out automatically.

### 2. CONSTRUCTION OF THE DEVICE

This time measuring device is made with CMOS integrated circuits, which feature working frequency above 10 MHz and low dissipated power. The measurement range is 0.1  $\mu$ s  $\div$  9.99 ms, divided in 0.1  $\mu$ s  $\div$  99.9  $\mu$ s, 100  $\mu$ s  $\div$  999  $\mu$ s and 1 ms  $\div$  9.99 ms sub-ranges. The overflowing of the 9.99 ms value is signaled by a red LED. The schematic block diagram is shown in fig.2, and the electronic diagram in fig.2.

The 10 MHz oscillator consists of gate  $U_{8B}$  (4001, quad NOR gates), quartz  $Y_1$  and the corresponding components, and the gate  $U_{8A}$  separates the oscillator from the rest of the device. The oscillator frequency can be adjusted at exactly 10.000 MHz by means of the ceramic trimmer capacitor  $C_1$ .

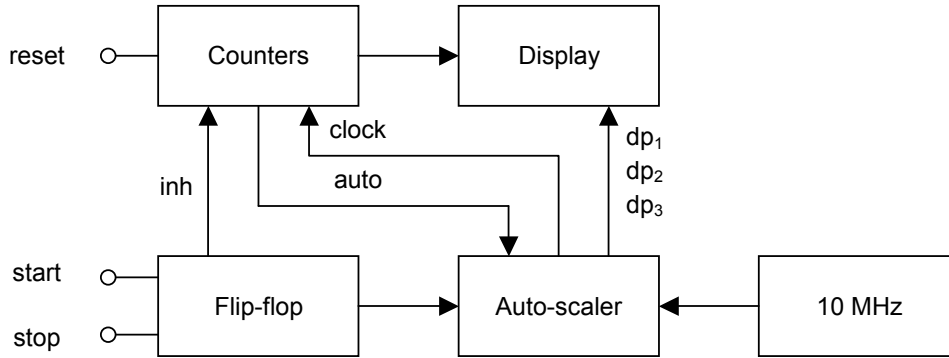


Fig.1. Schematic block diagram of the device.

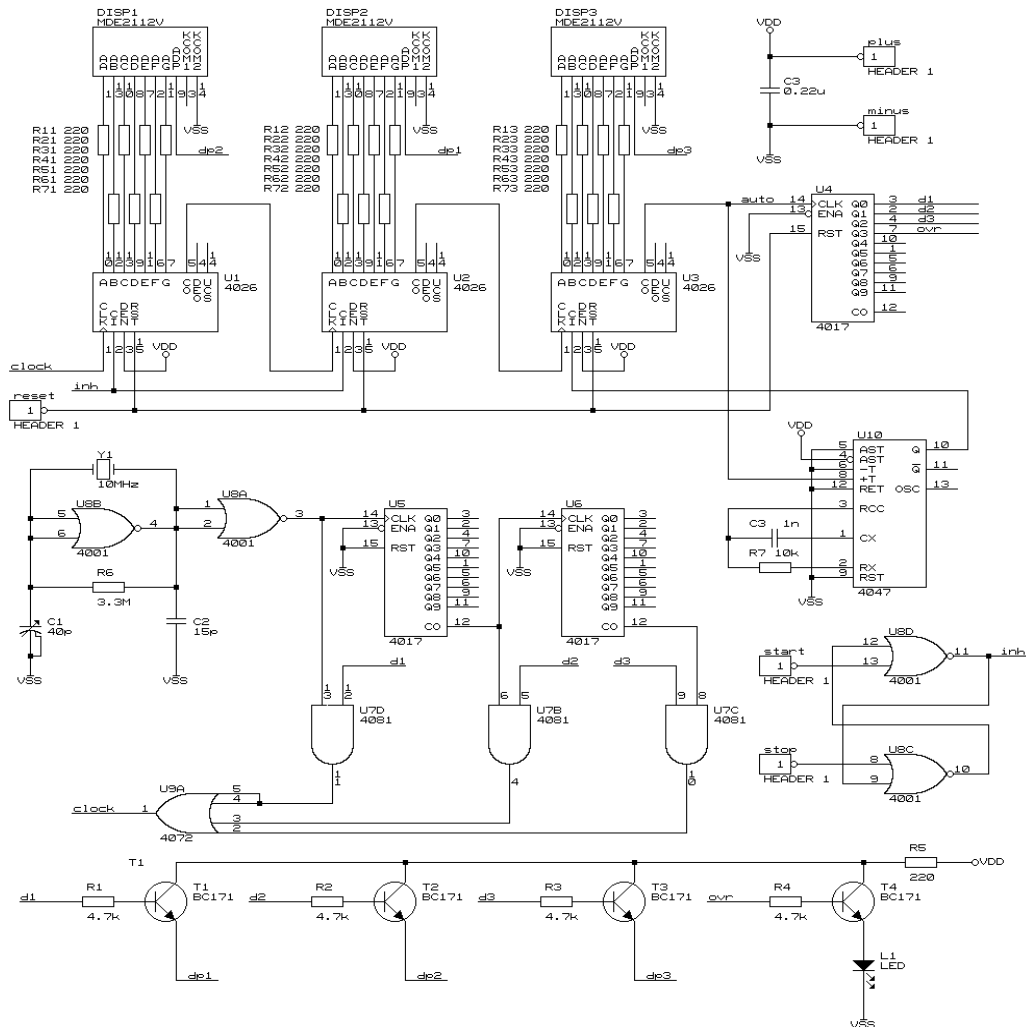


Fig.2. Electronic diagram of the device.

The auto-scaler block has several functions:

- o divides the 10 MHz signal by means of the circuits  $U_5$  and  $U_6$  (4017, decadic counter with decimal decoded outputs),

and supplies the 1 MHz and 100 kHz signals;

- o detects the overflowing of the current measuring range by means of circuit  $U_4$  (4017, decadic counter with decimal

decoded outputs); it counts the leading edges of the *auto* signal, which is emitted by the counters block at each zero of the last display while counting, ordering successively the signals  $d_1$ ,  $d_2$ ,  $d_3$  and *ovr* to become logic 1; the first three signals command the three measuring sub-ranges, and the fourth signals the overflowing of the last sub-range;

- selects and sends to the counters block the 10 MHz, 1 MHz and 100 kHz, according to the state of  $d_1$ ,  $d_2$  and  $d_3$  signals, by means of gates  $U_{7B,C,D}$  (4081, quad AND gates) and  $U_{9A}$  (4072, two 4-inputs OR gates); if signal *ovr* is at logic 1 ( $d_{1-3}$  at logic 0), then no signal is sent to the counters block;
- lights the decimal points, according to the current measuring sub-range, by means of transistors  $T_{1-3}$  and the corresponding components (signals  $dp_{1-3}$ ), and the “overflow” red LED, by means of transistor  $T_4$ .

The counters block has been realized with circuits  $U_{1-3}$  (4026, decadic counter with 7-segment decoded outputs), cascade-connected, and circuit U10 (4047, monostable/ astable multivibrator). The CARRY-OUT output of circuit  $U_3$  supplies the *auto* signal, worked by the auto-scaling block.

The same signal is taken by circuit U10, configured as monostable multivibrator; it supplies an  $0.3 \mu\text{s}$  pulse to the CARRY-IN input of circuit  $U_3$  and makes it advance with one unit, so that the new measuring range begins with 100, after the current range has finished at 999. The running of the counters block is validated if the *inh* signal is at logic 0, and the resetting is carried out if the *reset* external signal is at logic 1.

The display block is made of three LED displays  $DISP_{1-3}$  (MDE211V, 7-segment common cathode LED display) and LED  $L_1$ . The display segments are connected to the corresponding output pins of circuits  $U_{1-3}$  by means of current limitation resistors, and the decimal points and  $L_1$  are driven by the auto-scaling block.

The flip-flop block is made of gates  $U_{8C}$  and  $U_{8D}$  (4001, quad NOR gates) and is driven by the external signals *start* and *stop*. The output signal of this block is *inh*, which validates (logic 0) or inhibits (logic 1) the running of the next block.

### 3. FUNCTIONING OF THE DEVICE

The diagrams of the external signals start, stop and reset are shown in fig.3.

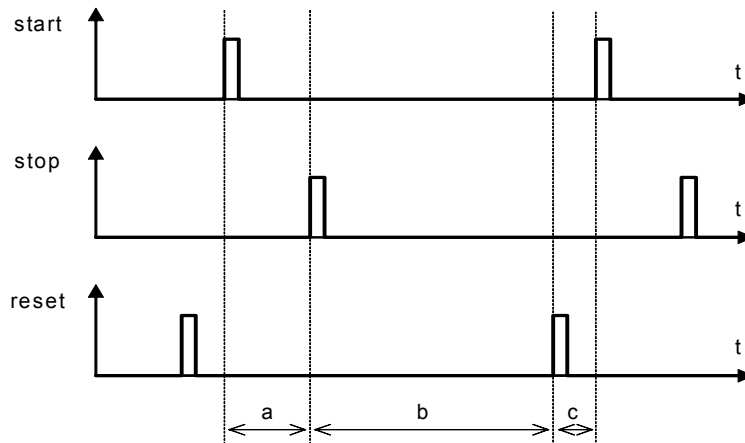


Fig.3. Diagrams of signals start, stop and reset; a – counting, b – displaying, c – resetting.

Before the measuring begins, the measuring device must be reset by means of a positive pulse at the RESET inlet. Initially, the  $Q_0$  output of circuit  $U_4$  is active, so signal  $d_1$  is at logic 1, which means we are in the first measuring sub-range  $0.1 \mu\text{s} \div 99.9 \mu\text{s}$ ;

the gates  $U_{7D}$  and  $U_{9A}$  select the 10 MHz clock signal and the decimal point of  $DISP_2$  is lit by means of transistor T1, so the display shows „00.0“. When a positive pulse arrives at inlet START, the flip-flop makes the *inh* signal change at logic 0, allowing the

counters block to count the 10 MHz pulses, that is the tenths of microsecond.

If there wasn't any positive pulse at inlet *STOP* until  $99.9 \mu\text{s}$  had passed, circuit  $U_3$  goes from "9" to "0" and changes the *auto* signal at logic 1; this leading edge makes active the output  $Q_1$  of circuit  $U_4$ , so signal  $d_2$  changes to logic 1, which means we have passed to the second measuring sub-range  $100 \mu\text{s} \div 999 \mu\text{s}$ ; the 1 MHz signal is selected by means of gates  $U_{7B}$  and  $U_{9A}$  and the decimal point of  $DISP_1$  is lit by means of transistor  $T_2$ ; the same leading edge of signal *auto* activates the monostable  $U_{10}$ , which makes  $U_3$  advance from "0" to "1", so the display shows "100." and the counters block will count the microseconds.

If still there was no positive pulse at inlet *STOP* until  $999 \mu\text{s}$  have passed, the device similarly passes to the third measuring sub-range  $1 \text{ ms} \div 9.99 \text{ ms}$ ; the 100 kHz signal is selected, the decimal point of  $DISP_3$  is lit, so the display shows "1.00", and the tens of microseconds are counted.

If there wasn't any positive pulse at inlet *STOP* until 9.99 ms have passed, the *auto* signal goes again at logic 1, causing the activation of output  $Q_3$  of circuit  $U_4$ ; thus, the *ovr* signal changes at logic 1 and the overflow red LED  $L_1$  is lit by means of transistor  $T_4$ . Signals  $d_{1-3}$  are all at logic 0, the decimal points are all switched off and no signal passes to the counters block, so the display shows "☼100", meaning "overflow".

If a positive pulse arrives at inlet *STOP* until 9.99 ms from the positive pulse at inlet *START*, then the  $U_{8C} - U_{8D}$  flip-flop changes the *inh* signal to logic 1, thus inhibiting the counters block, so that the display "freezes" at the counted value, its measuring unit being given by the position of the decimal point. So the device has counted the microseconds (the second or the first decimal points are lit) or the milliseconds (the third decimal point is lit) that have passed between the leading edges of the *start* and *stop* signals.

In order to insure a comfortable reading, it is advisable that the external *reset* signal should be delayed with about 1 s after the leading edge of the external *stop* signal.

#### 4. CONCLUSIONS

One major advantage of this device is the comfortable use, without any manual switching between the measuring sub-ranges. Another advantage consists in the use of a quartz-driven clock generator, which implies far better accuracies compared to other time measuring methods. The reading of the values is simplified by using only three 7-segment displays and by the positions of the decimal points.

This device can be used in tandem with a classic CRT flaw detector or even as a standalone block, together with the emission-reception ultrasonic assemblies. Also, it can be used for measuring other short time intervals, mainly if the events are relatively periodical; for example, if the *reset* signal is properly automated, this device can be used as a period-meter.

With minimal adaptations, this device can be used as frequency-meter or as particle counter if provided with proper transducers. According to the interest domain, many other uses for this device can be found; for example, the device can be extended for maximum 9 measurement sub-ranges, by completing the auto-scaling block with another 4017 counters for dividing the initial 10 MHz signal and the corresponding selection gates, driven by the outputs of counter  $U_4$ , and further LED's should be added in order to clearly show the current sub-range.

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