CONDUCTION MECHANISMS IN MIS STRUCTURES WITH HIGH-K INSULATOR LAYERS

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ABSTRACT:

High-k $La_2Hf_2O_7$ traps in insulator layers deposited on Silicon were characterized using temperature dependent I-V, C-V and photocurrent measurements on MIS structures. In addition, the temporal response following a voltage step was used to give insight into the influence of traps on the electrical characteristics of the device. In structures with thicker insulator layers the energy-band diagram is close to the one deduced theoretically from the difference between the work-functions of Al and Si. However, at temperatures lower than 260 K the C-V curves move towards positive voltages due to the increased number of negatively charged centers. We attribute the increase of the concentration of negatively charged centers that we observe when the temperature is decreased to the presence of strain in the structure.

KEYWORDS: Conducting phenomena in semiconductors and insulators, Electronic transport in interface structures

1. INTRODUCTION

High-k dielectrics are of considerable interest due to their potential to replace SiO_2 in the gate of future transistor. Here we investigate high-k $La_2Hf_2O_7$ insulator layers deposited by MBE on n-Silicon. For these structures the work-function of Al is lower than that of n-Si, allowing, in the ideal case, the appearance of an accumulation layer in Silicon and in consequence of two injecting contacts for both sign of the biasing voltage. I-V, C-V, photocurrent measurements and temporal response following a voltage step were used for characterization. Table 1 summarizes the details related to the grown oxide layers on n-type Si.

Table 1 Details of the high-k oxide layers grown on n-Si

Sample	Intended thickness (nm)	Measured thickness (nm)
MBE 448	10 nm	11.2 nm
MBE 449	20 nm	23 nm
MBE 450	40 nm	48.7 nm

2. C-V MEASUREMENTS

Fig. 1 shows typical high frequency C-V curves measured at different temperatures for samples MBE 449 and MBE 450.

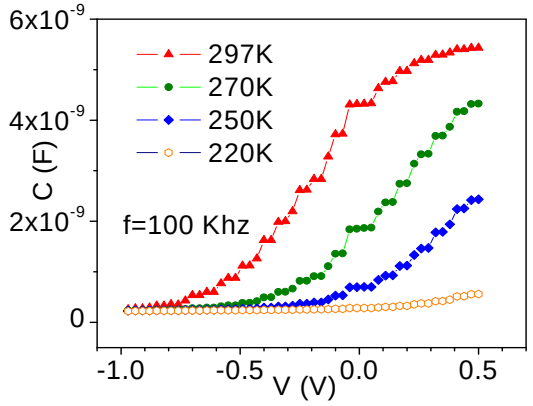

Fig. 1. Typical high frequency (100 kHz) C-V curves measured at different temperatures for samples MBE 449 and MBE 450

At room temperature the Flat-Band-Voltage is about -0.15 eV, value that is very close to that corresponding to the ideal Al-n-Si pair.

However, by lowering the temperature a significant shift of the C-V characteristics

towards positive voltages is observed. This shift indicates the appearance of a high concentration of negatively charged centers in the insulator layer and/or at the interface. In the same time, at low temperatures, the structure is in inversion for the investigated applied voltages (-1V ¸ +1V).

At low temperatures there is a barrier (in Silicon) for electron injection in the insulator and the Fermi level is pinned near the valence band of Silicon. This latter aspect is determined by the increase of the insulator/silicon interface state density. This increase and the corresponding shift of the Fermi level, observed at first in C-V characteristics, was evidenced also by Conductance-Voltage (G-V) measurements at different frequencies and temperatures, using the method proposed by Hill [1].

Unfortunately, we are able to prove this only qualitatively because our experimental setup allows the use of only four frequencies. Even so, we found from the four available points that the maximum value of the density of interface states increases and moves towards the valence band edge as the temperature lowers. This aspect results from Table 2 according to the values determined at two temperatures for which clear G maximums were obtained:

Table 2 Density of states computed using the Hill method

Temperature	Density of states	Position relative to the conduction band edge
297 K	4×10^{12} $cm^{-2}eV^{-1}$	-0.1 eV
250 K	1.85×10^{13} $cm^{-2}eV^{-1}$	-0.54 eV

A completely different situation is observed for structures with much thinner insulator layers (see Fig. 2 for MBE 448 sample). In this case, the C-V curves are shifted towards more negatively voltages comparatively with the ideal curve. For an applied voltage between -1 V and + 1 V, the structure is in an accumulation for any temperature, suggesting that from the point of view of electron injection, the structure is symmetrical from both sides.

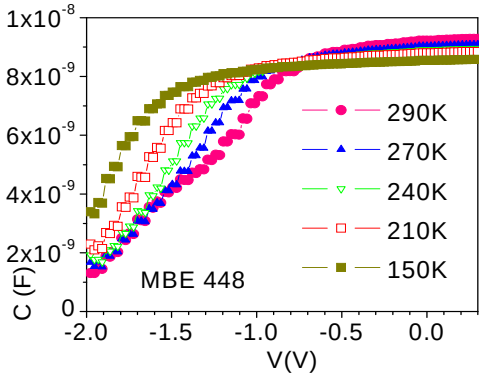

Fig. 2. Typical high frequency (100 kHz) C-V curves measured at different temperatures for sample MBE 448

3. I-V MEASUREMENTS

Fig. 3 shows the I-V characteristics for the MBE 449 and MBE 450 samples.

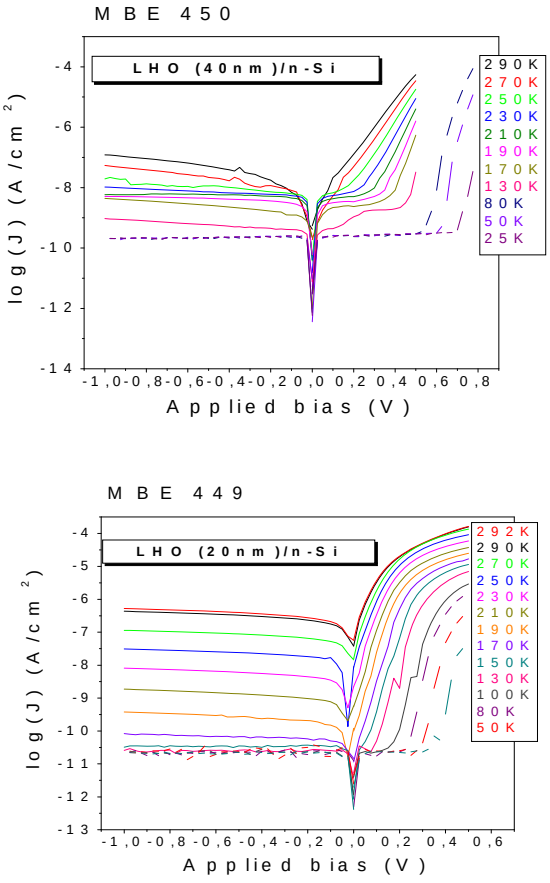

Fig. 3. I-V characteristic of samples MBE 449 and MBE 450

The electron injection is possible from both sides, even if the voltage drop on the insulator layer is higher for the positive bias than for the negative one, resulting in an asymmetrical behavior of the current flow. At lower temperatures, a barrier is present in the Silicon side hindering the electron injection from both sides.

Fig. 4 shows the I-V characteristics of sample MBE 448 for different temperatures.

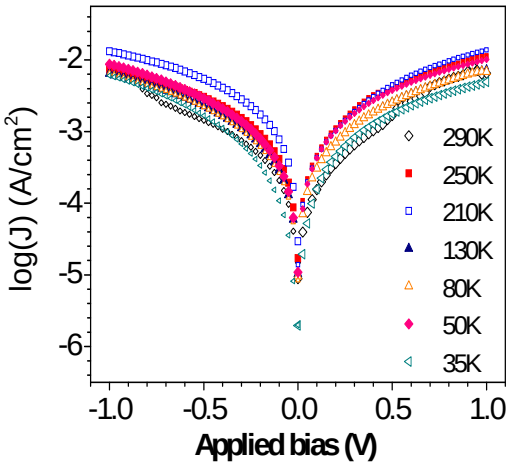

Fig. 4. I-V characteristics of sample MBE 448 for different temperatures

We have shown above that the MBE 448 sample presents symmetrical conditions for electron injection from both sides for all temperatures. Therefore symmetrical I-V characteristics are expected, as were indeed observed.

4. PHOTOCURRENT MEASUREMENTS

Photoelectrical measurements demonstrate a significant photo-current for photon energies larger than 1.1 eV (see Fig. 5), corresponding to the Silicon energy gap.

This can only happen if the carriers are directly injected into the insulator layer, after the electron-hole pair created in Silicon is separated by the field in this region. This suggests the presence of "impurity channels" in the insulator, making possible the flow of both electrons and holes. The carrier injection over the contact barriers for both electrons and holes can take place only at much higher photon energies, as indicated in Fig. 5.

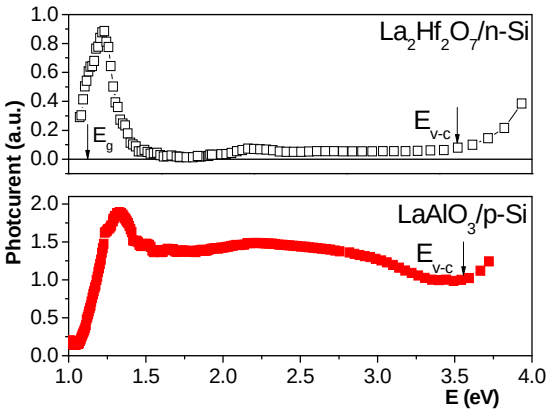

Fig. 5. Photocurrent in high-k MOS structures having the insulator layer deposited on both p-type and n-type Si

We took into account two kinds of impurity centers. The first type allows the transport of electrons and holes while the second type acts as a carrier trap. The modeling of the gate current behavior shows that the current is limited by the space charge injected into the impurity band [2]. However, this SCL current is drastically influenced by the presence of the deep traps. Thus, at low temperatures we evidenced the abrupt transition that happens when the quasi-Fermi-level is lowered and crosses over trap levels (Fig. 6). This ladder shape of the I-V curve is characteristic for the SCL currents in the insulators with traps [2].

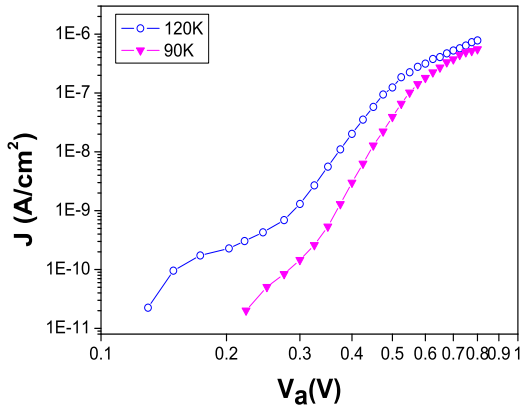

Fig. 6. I – V characteristics of a $La_2Hf_2O_7$ based MOS structure illustrating the ladder behavior at low temperatures

5. Temporal response following a voltage step

The presence of these deep traps is also directly evidenced by the time behavior of the gate current (Fig. 7).

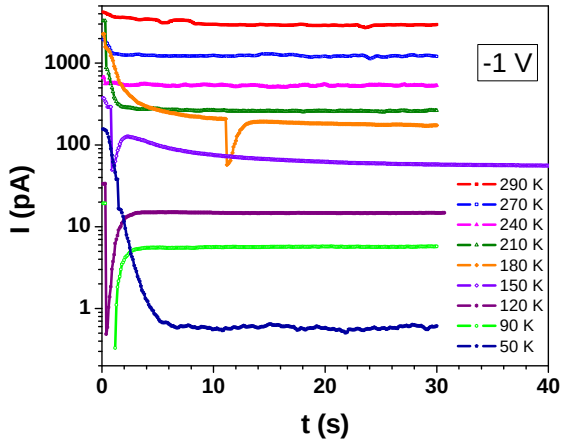

Fig. 7. Time dependence of currents measured for the $La_2Hf_2O_7$ MOS structure at different temperatures for -1V applied bias.

The current density at a given voltage is controlled by both the carrier mobility and by the filling of traps. The steady-state value is reached with the characteristic time constant of the trapping process. The problem was theoretically investigated by Many and Rakavy [3] and they found an exponential law for the current decay in time. Indeed, we found experimentally that the currents decay exponentially with time constants of the order of seconds. Another interesting aspect connected with the presence of traps is the oscillatory behavior of the gate current when the Fermi level crosses a trap level (Fig. 8).

We have no direct information about the origin of the centers that create the impurity band in which the electrons move. Taking into account new results reported in literature [4], the most important fact that influences the high–k insulator conductivity is the oxygen pressure during layer deposition. If the pressure is high, the conductivity is low.

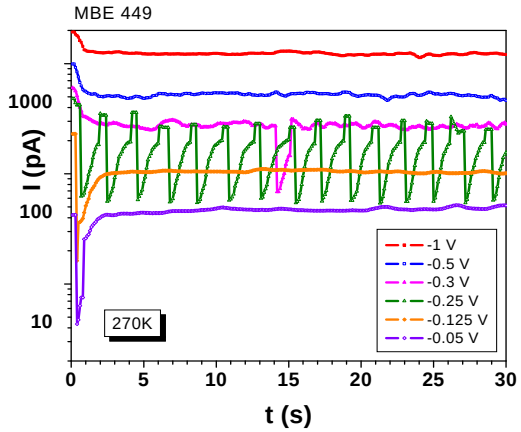

Fig. 8. The time dependence of currents for different applied voltages

Therefore, we suppose that the most important center involved in the electron transport is determined by an oxygen vacancy. It can hold two electrons with opposite spins. Another captured electron, as a consequence of injection, suffers a Hubbard interaction and an upper level is formed. Thus, the holes can move in the lower Hubbard band and electrons in the upper one. This model can explain the carrier transport in both types of structures (oxide/Si-p or Si-n) by the presence of two leakage channels in the insulator, close to the silicon conduction and valence bands respectively. It is well known that the presence of deep traps is expected in amorphous materials.

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